FIG. 1

MODULE	STATE COVERAGE	BRANCH COVERAGE	• • •	TOGGLE COVERAGE
TOTAL	95.7% 1231/1286 (55)			
• • •				
Abcd	94.9% 148/156 (8)			
• •				

FIG. 2

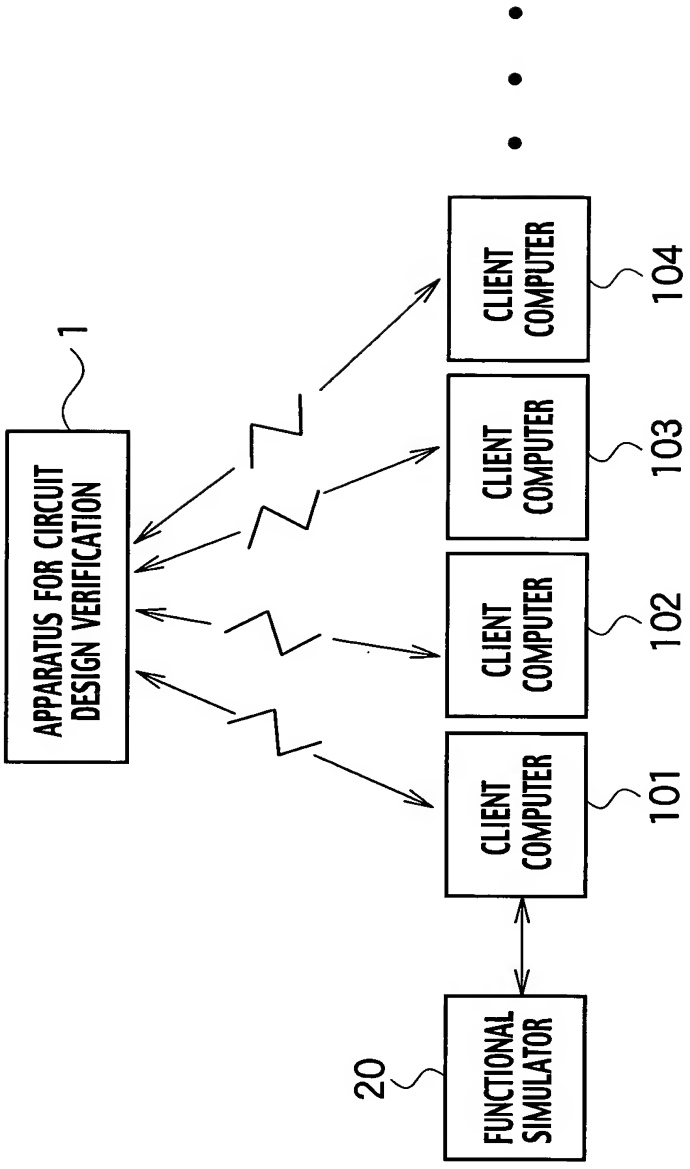

APPARATUS FOR CIRCUIT DESIGN VERIFICATION
1
CLIENT COMPUTER
101
CLIENT COMPUTER
102
CLIENT COMPUTER
103
CLIENT COMPUTER
104
FUNCTIONAL SIMULATOR
20

FIG. 3

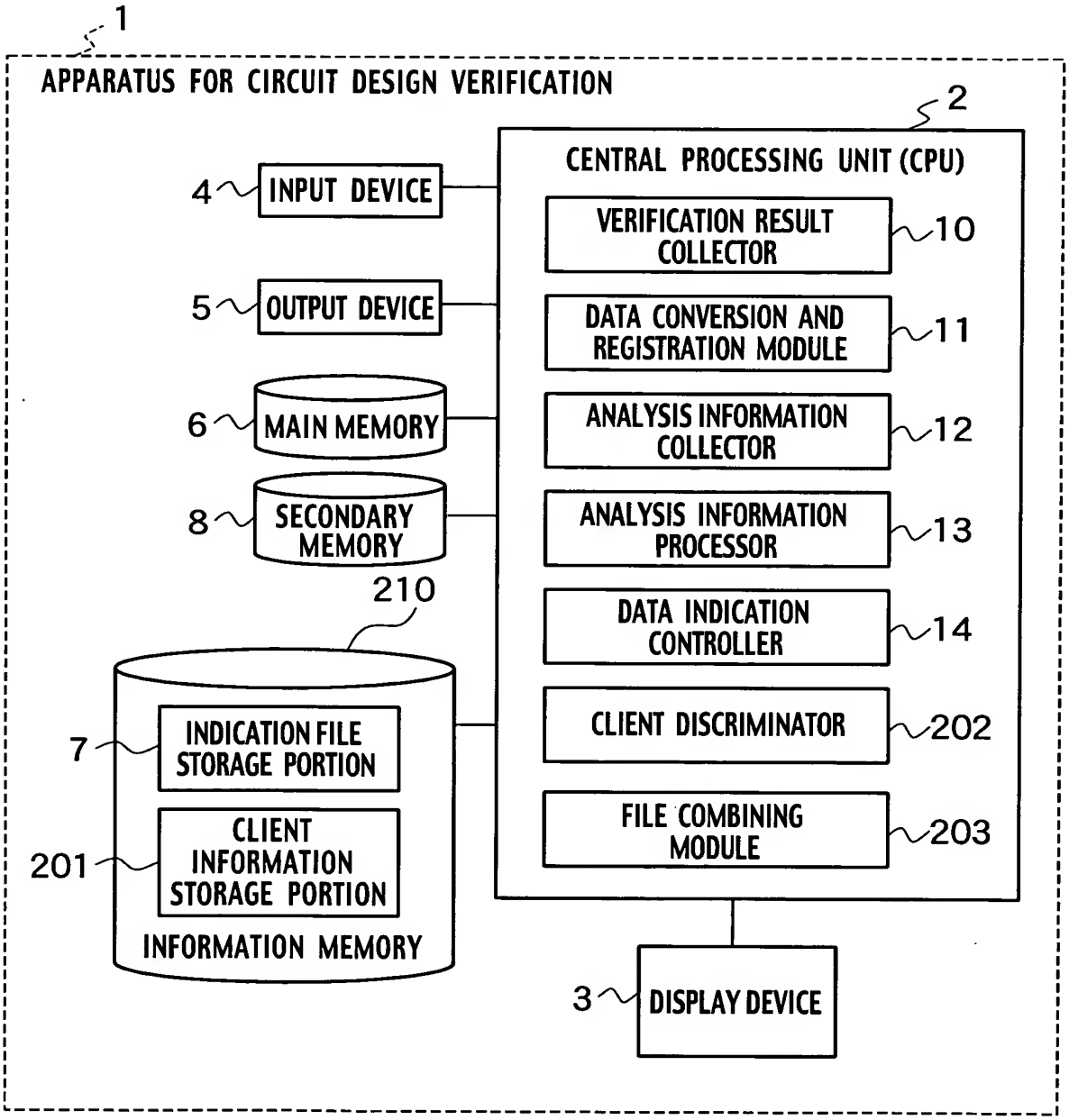

1
APPARATUS FOR CIRCUIT DESIGN VERIFICATION
2
CENTRAL PROCESSING UNIT (CPU)
4
INPUT DEVICE
5
OUTPUT DEVICE
6
MAIN MEMORY
8
SECONDARY MEMORY
210
7
INDICATION FILE STORAGE PORTION
201
CLIENT INFORMATION STORAGE PORTION
INFORMATION MEMORY
VERIFICATION RESULT COLLECTOR
10
DATA CONVERSION AND REGISTRATION MODULE
11
ANALYSIS INFORMATION COLLECTOR
12
ANALYSIS INFORMATION PROCESSOR
13
DATA INDICATION CONTROLLER
14
CLIENT DISCRIMINATOR
202
FILE COMBINING MODULE
203
3
DISPLAY DEVICE

FIG. 4

PRODUCT NAME	REGISTRATION DATES
aaaaa	1999/09/24
bbbbb	1999/09/28
•	
•	
•	

FIG. 5

QUALITY RANK	: A (2001.12.19)
RTL CODE COVERAGE TOOL VERSION	: 6.000
RTL SIMULATOR	: Verilog-XLx.x
RELATED INFORMATION	

FIG. 6

PRODUCT NAME : aaaaa
VERSION :
CONTAINING IP NAME,
PRESENCE OF UNVERIFIED FUNCTION, RANK :
TEST PATTERN
TYPE : TSTL2
VERSION :
DEPARTMENT :
PERSON IN CHARGE :
CONTACT ADDRESS :

FIG. 7

MODULE	STATE COVERAGE		BRANCH COVERAGE		• • •	TOGGLE COVERAGE	
	PRE-ANALYSIS RESULT	ANALYSIS RESULT	PRE-ANALYSIS RESULT	ANALYSIS RESULT		PRE-ANALYSIS RESULT	ANALYSIS RESULT
TOTAL	95.7% 1231/1286 (55)	97.5% 1254/1286 (10+8+5/55)					
• • •							
Abcd	94.9% 148/156 (8)	98.0% 153/156 (2+2+1/8)					
• •							

FIG. 8

SERIAL NUMBER	LINE NUMBER	CORRESPONDING RTL DESCRIPTION	ANALYSIS RESULT					
			EXCLUDED BECAUSE OF UNUSED FUNCTION	EXCLUDED BECAUSE OF REDUNDANT DUE TO SPECIFIC TOOL	EXCLUDED BECAUSE OF INTENTIONAL REDUNDANT FOR EASY READING	UN-EXCLUDED BECAUSE OF INSUFFICIENT VERIFICATION PATTERN	UN-EXCLUDED BECAUSE OF INSUFFICIENT ANALYSIS	DETAILED COMMENT
1	418		V					
2	721			V				DEFAULT DESCRIPTION CORRESPONDING TO SYNOPYS DC
3	1083						V	
4	1156				V			
N	2023					V		

X PORTIONS y PORTIONS z PORTIONS w PORTIONS

FIG. 9

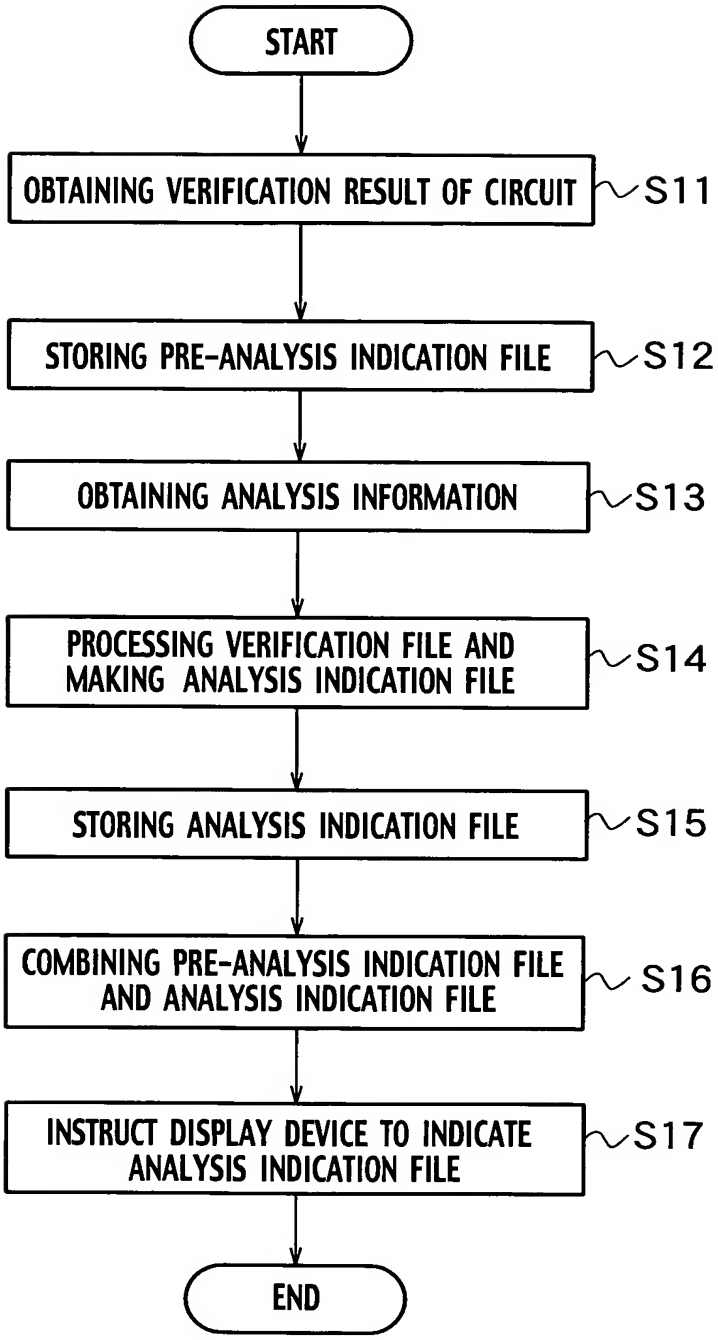

START
OBTAINING VERIFICATION RESULT OF CIRCUIT
S11
STORING PRE-ANALYSIS INDICATION FILE
S12
OBTAINING ANALYSIS INFORMATION
S13
PROCESSING VERIFICATION FILE AND MAKING ANALYSIS INDICATION FILE
S14
STORING ANALYSIS INDICATION FILE
S15
COMBINING PRE-ANALYSIS INDICATION FILE AND ANALYSIS INDICATION FILE
S16
INSTRUCT DISPLAY DEVICE TO INDICATE ANALYSIS INDICATION FILE
S17
END

FIG. 10

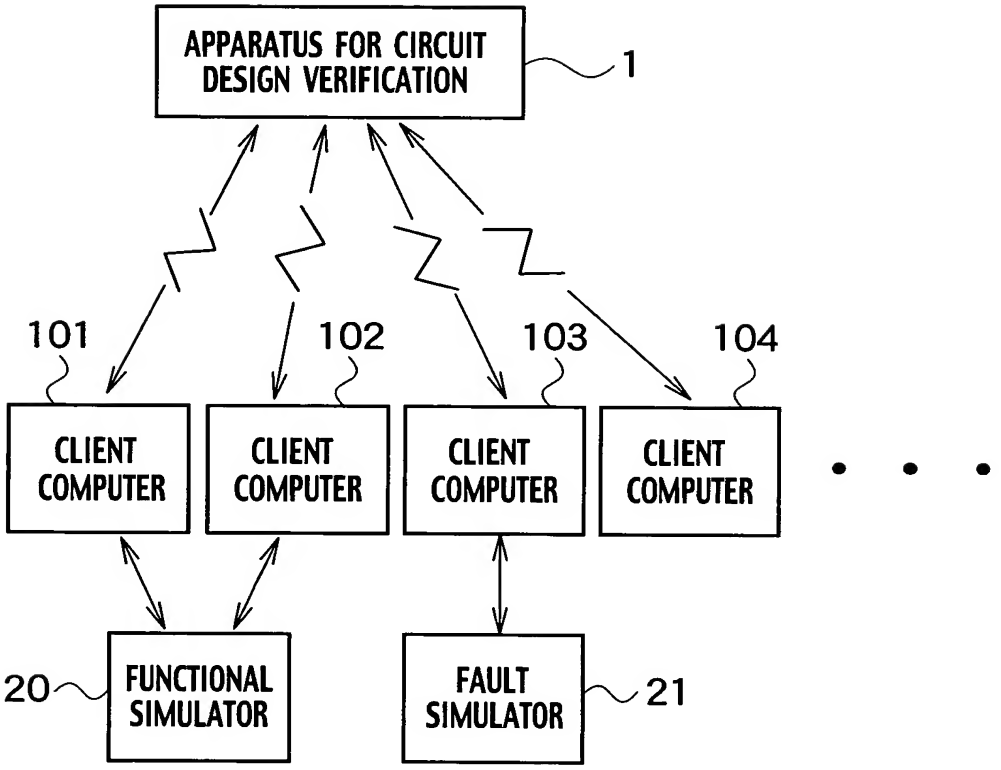

APPARATUS FOR CIRCUIT DESIGN VERIFICATION
1
101
102
103
104
CLIENT COMPUTER
CLIENT COMPUTER
CLIENT COMPUTER
CLIENT COMPUTER
20
FUNCTIONAL SIMULATOR
FAULT SIMULATOR
21

FIG. 11

MODULE	STATE COVERAGE		BRANCH COVERAGE		• • •	FAULT COVERAGE	
	PRE-ANALYSIS RESULT	ANALYSIS RESULT	PRE-ANALYSIS RESULT	ANALYSIS RESULT		PRE-ANALYSIS RESULT	ANALYSIS RESULT
TOTAL	95.7% 1231/1286 (55)	97.5% 1254/1286 (10+8+5/55)					
• • •							
Abcd	94.9% 148/156 (8)	98.0% 153/156 (2+3/8)				93.2% 2983/3201 (218)	95.2% 3047/3201 (39+25/218)
• •							

FIG. 12

SERIAL NUMBER	FAULT LIST	NODE	ANALYSIS RESULT			
			EXCLUDED BECAUSE OF UNUSED FUNCTION	EXCLUDED BECAUSE OF OTHER REASONS	UN-EXCLUDED	DETAILED COMMENT
1	sa0	Abcd/xyyz[1]	V			
2	sa1	Abcd/awg		V		REDUNDANT FAULT
3	sa1	Abcd/wggza			V	INSUFFICIENT VERIFICATION PATTERN
N	sa0	Abcd/zxz	V			XXXX FUNCTION IS UNUSED

X PORTIONS

y PORTIONS

FIG. 13

SERIAL NUMBER	FAULT LIST	NODE	WEIGHT	ANALYSIS RESULT			
				EXCLUDED BECAUSE OF UNUSED FUNCTION	EXCLUDED BECAUSE OF OTHER REASONS	UN-EXCLUDED	DETAILED COMMENT
1	sa0	Abcd/xyyz[1]	237	V			
2	sa1	Abcd/awg	201		V		REDUNDANT FAULT
3	sa1	Abcd/wggza	127			V	INSUFFICIENT VERIFICATION PATTERN
N	sa0	Abcd/xz	20	V			XXXX FUNCTION IS UNUSED

X PORTIONS y PORTIONS

FIG. 14

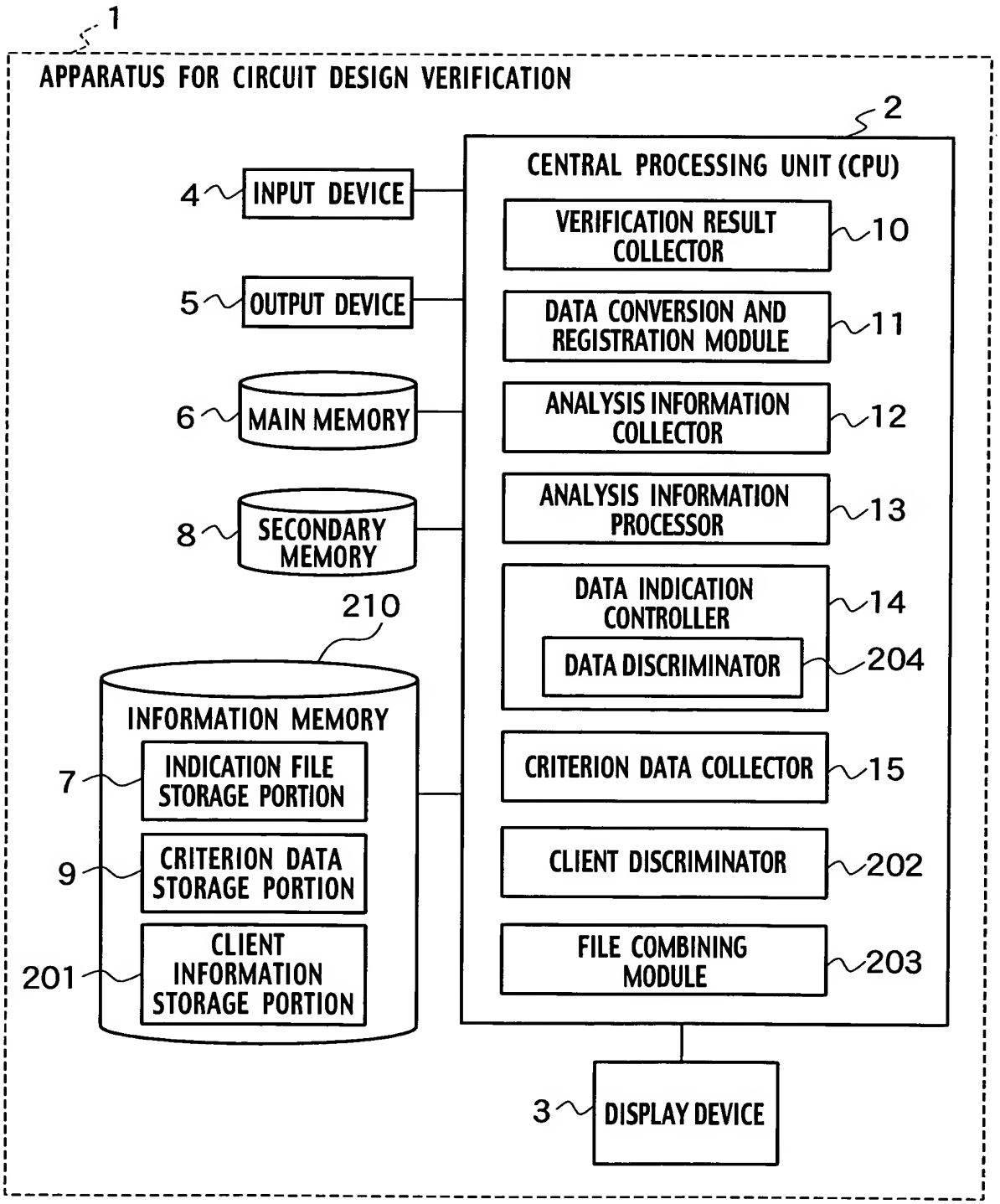

1
APPARATUS FOR CIRCUIT DESIGN VERIFICATION
2
CENTRAL PROCESSING UNIT (CPU)
4
INPUT DEVICE
5
OUTPUT DEVICE
6
MAIN MEMORY
8
SECONDARY MEMORY
210
INFORMATION MEMORY
7
INDICATION FILE STORAGE PORTION
9
CRITERION DATA STORAGE PORTION
201
CLIENT INFORMATION STORAGE PORTION
VERIFICATION RESULT COLLECTOR
10
DATA CONVERSION AND REGISTRATION MODULE
11
ANALYSIS INFORMATION COLLECTOR
12
ANALYSIS INFORMATION PROCESSOR
13
DATA INDICATION CONTROLLER
14
DATA DISCRIMINATOR
204
CRITERION DATA COLLECTOR
15
CLIENT DISCRIMINATOR
202
FILE COMBINING MODULE
203
3
DISPLAY DEVICE

FIG. 15

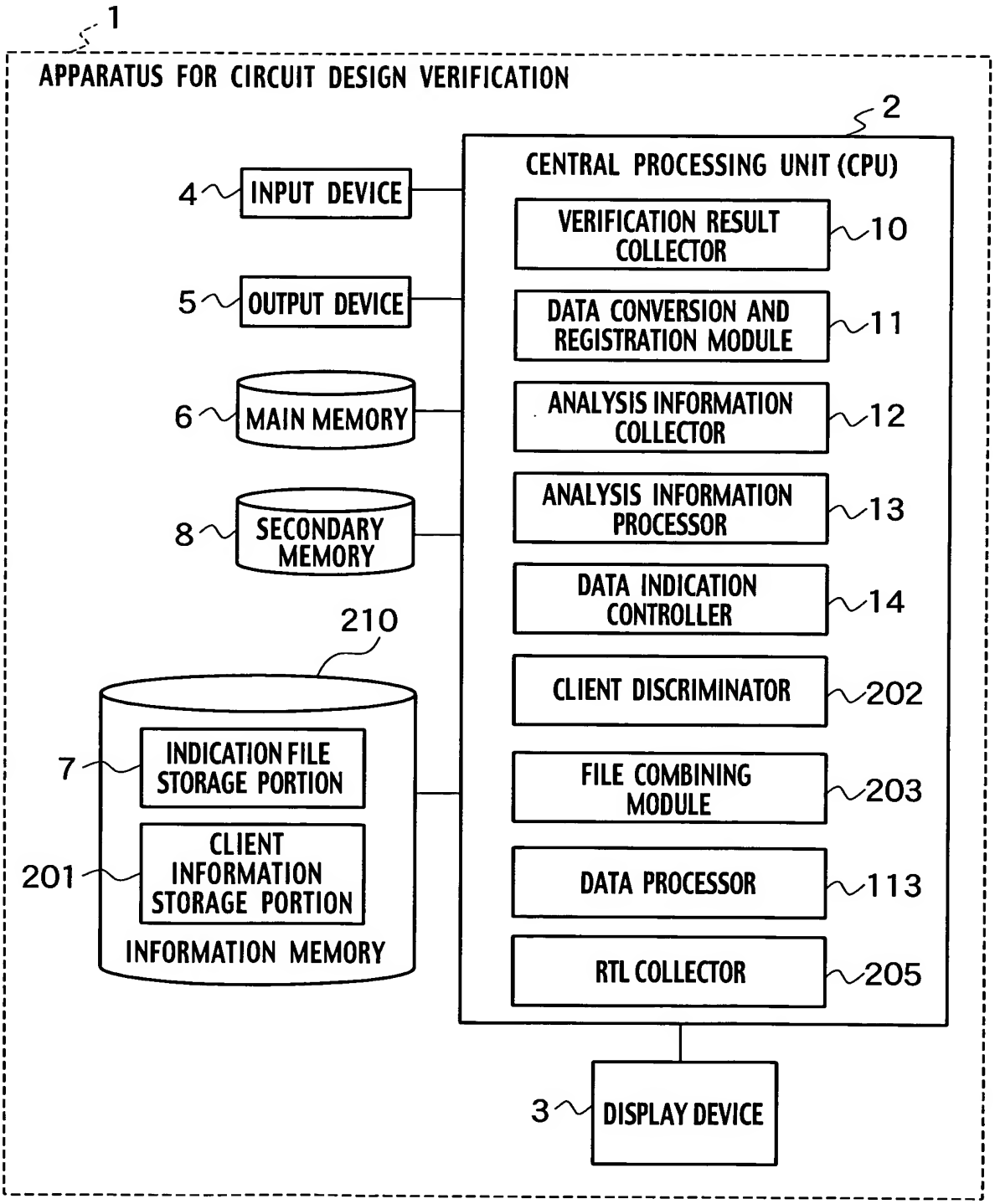

1
APPARATUS FOR CIRCUIT DESIGN VERIFICATION
2
CENTRAL PROCESSING UNIT (CPU)
4
INPUT DEVICE
5
OUTPUT DEVICE
6
MAIN MEMORY
8
SECONDARY MEMORY
210
7
INDICATION FILE STORAGE PORTION
201
CLIENT INFORMATION STORAGE PORTION
INFORMATION MEMORY
VERIFICATION RESULT COLLECTOR
10
DATA CONVERSION AND REGISTRATION MODULE
11
ANALYSIS INFORMATION COLLECTOR
12
ANALYSIS INFORMATION PROCESSOR
13
DATA INDICATION CONTROLLER
14
CLIENT DISCRIMINATOR
202
FILE COMBINING MODULE
203
DATA PROCESSOR
113
RTL COLLECTOR
205
3
DISPLAY DEVICE

FIG. 16

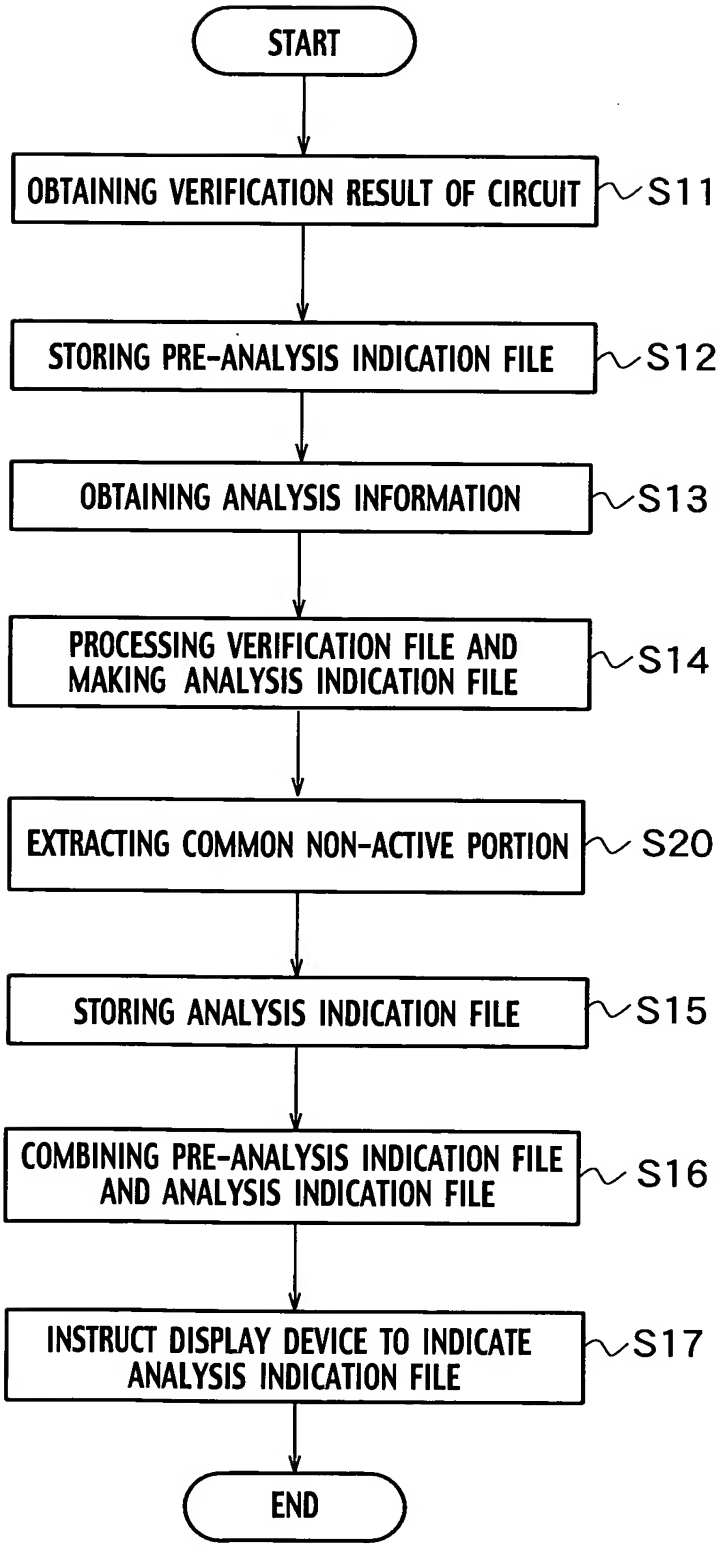

START
OBTAINING VERIFICATION RESULT OF CIRCUIT
S11
STORING PRE-ANALYSIS INDICATION FILE
S12
OBTAINING ANALYSIS INFORMATION
S13
PROCESSING VERIFICATION FILE AND MAKING ANALYSIS INDICATION FILE
S14
EXTRACTING COMMON NON-ACTIVE PORTION
S20
STORING ANALYSIS INDICATION FILE
S15
COMBINING PRE-ANALYSIS INDICATION FILE AND ANALYSIS INDICATION FILE
S16
INSTRUCT DISPLAY DEVICE TO INDICATE ANALYSIS INDICATION FILE
S17
END

FIG. 17

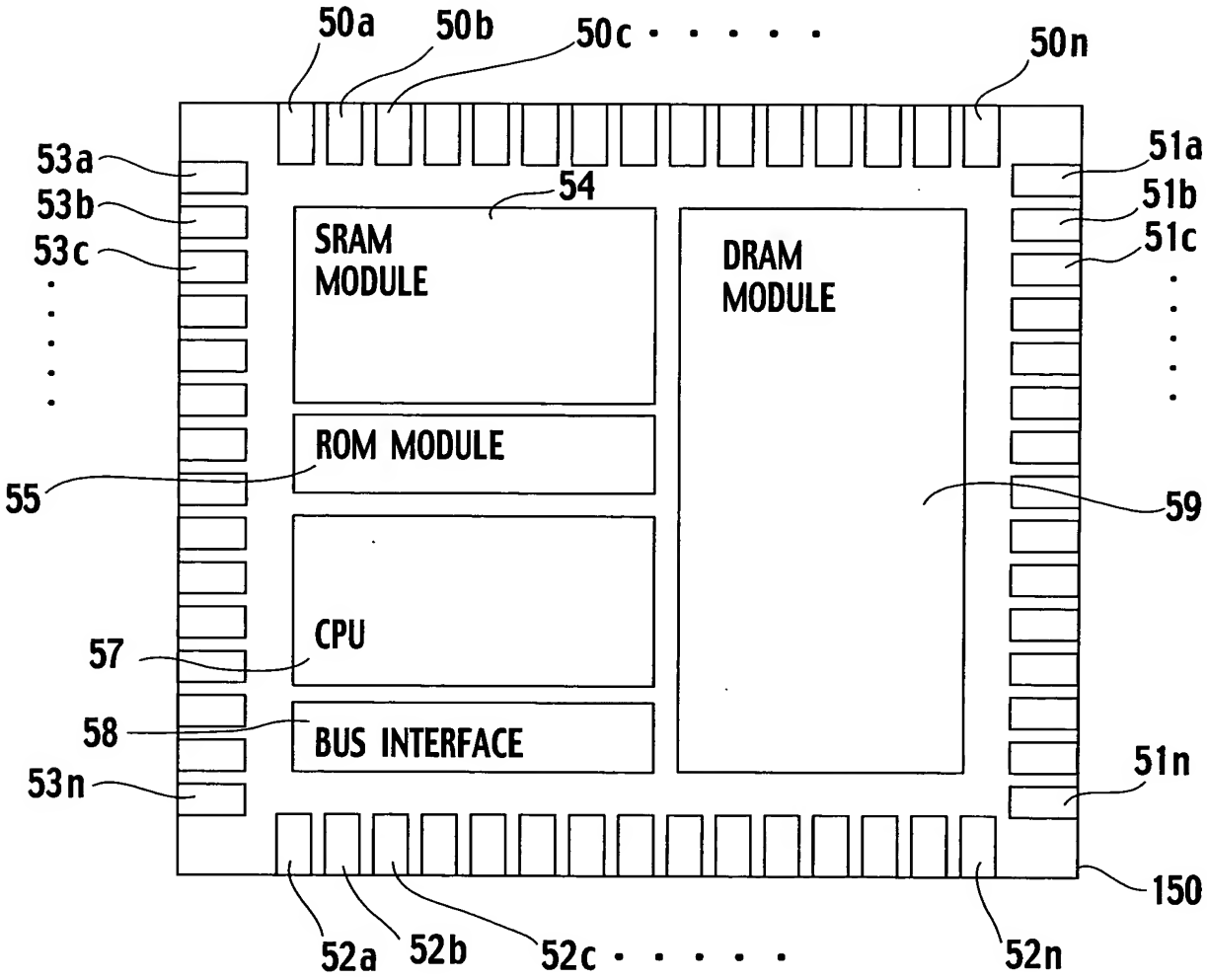
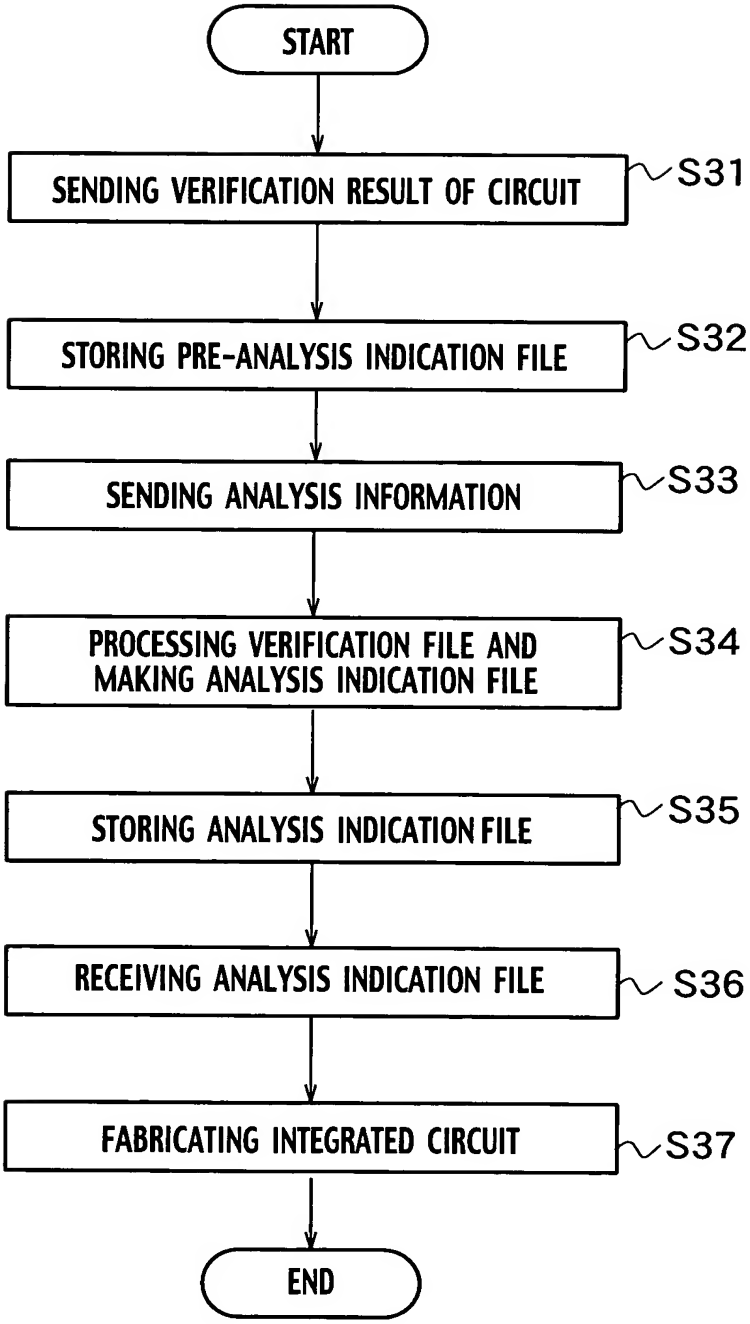

50a
50b
50c
50n
53a
53b
53c
53n
54
SRAM MODULE
DRAM MODULE
ROM MODULE
CPU
BUS INTERFACE
55
57
58
59
51a
51b
51c
51n
150
52a
52b
52c
52n

FIG. 18


START
SENDING VERIFICATION RESULT OF CIRCUIT
S31
STORING PRE-ANALYSIS INDICATION FILE
S32
SENDING ANALYSIS INFORMATION
S33
PROCESSING VERIFICATION FILE AND MAKING ANALYSIS INDICATION FILE
S34
STORING ANALYSIS INDICATION FILE
S35
RECEIVING ANALYSIS INDICATION FILE
S36
FABRICATING INTEGRATED CIRCUIT
S37
END